DelGrad: Exact gradients in spiking networks for learning transmission delays and weights

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Abstract

Spiking neural networks (SNNs) inherently rely on the timing of signals for representing and processing information. Transmission delays play an important role in shaping these temporal characteristics. Recent work has demonstrated the substantial advantages of learning these delays along with synaptic weights, both in terms of accuracy and memory efficiency. However, these approaches suffer from drawbacks in terms of precision and efficiency, as they operate in discrete time and with approximate gradients, while also requiring membrane potential recordings for calculating parameter updates. To alleviate these issues, we propose an analytical approach for calculating exact loss gradients with respect to both synaptic weights and delays in an event-based fashion. The inclusion of delays emerges naturally within our proposed formalism, enriching the model’s search space with a temporal dimension. Our algorithm is purely based on the timing of individual spikes and does not require access to other variables such as membrane potentials. We explicitly compare the impact on accuracy and parameter efficiency of different types of delays – axonal, dendritic and synaptic. Furthermore, while previous work on learnable delays in SNNs has been mostly confined to software simulations, we demonstrate the functionality and benefits of our approach on the BrainScaleS-2 neuromorphic platform.

1 Introduction

The mammalian brain has always represented the ultimate example of computational prowess, and therefore remains an important source of inspiration for understanding intelligence and replicating it in artificial substrates. In particular, its specific mechanisms for transmitting and processing information have been the subject of intense scrutiny and debate. Among these, the pulsed communication between neurons, predominantly based on all-or-none events called action potentials or spikes, stands out as a distinguishing feature, and has thus been suggested to play an important role in the brain’s remarkable combination of computational performance and energy efficiency [1, 2]. Consequently, spike-based communication represents a de-facto standard across current neuromorphic platforms, which aim to inherit the proficiency of their biological archetype by replicating chosen aspects of its structure and dynamics [3–7].

Among the various encoding schemes proposed for spiking neurons, the representation of information within the specific timing of individual spikes is of particular interest [8], as it effectively allows the communication of real numbers on the energy budget for generating and transmitting a single bit. However, such an implicit representation is more difficult to learn than the more explicit, rate-based representation in conventional neural networks. This gives rise to a specific call for SNN training algorithms that exploit the temporal richness of spike timing codes for solving computational tasks efficiently and accurately, while remaining capable of operating under the realistic constraints of the underlying physical substrate, whether biological or artificial.

Recent years have seen an exciting trend in this direction, showing how the performance of SNNs can be improved by optimizing various temporal parameters. Such parameters include neuronal integration time constants [9–14], adaptation time constants [15], and delay variables [16–18]. In particular, spike transmission delays have been suggested to significantly enrich the information processing capabilities of spiking networks [19, 20], but specific applications to computationally demanding tasks have long since remained an open issue. Lately however, there has been mounting
Figure 1: Information flow in an SNN. a) Network architecture of a feed-forward SNN with a spiking input layer at the bottom, a hidden layer in the middle and the output layer on top. b) Zoom-in on the information processing in a single leaky integrate-and-fire (LIF) neuron in the hidden layer. Incoming spikes (blue, bottom) are integrated by the neuron’s membrane $u_m$ and generate postsynaptic potentials (PSPs), which accumulate additively. Once the membrane potential passes a threshold (grey dashed line), an output spike (orange, top) is generated and passed on to the neurons in the next layer. The PSP amplitudes are modulated by the respective synaptic weights $w$ (vertical red arrow); these are the parameters that are conventionally adapted during learning. Learnable transmission delays $d$ (horizontal red arrow) shift PSPs in time, providing additional temporal processing power to the neuron. c) Zoom-out to a raster plot of the full spiking activity in the network. The information passed between the layers is encoded in the timing of the spikes. The spike output of the network is decoded with a TTFS scheme: in the case of a classification task, the output neuron which generates the first output spike is indicative of the class to which the input belongs.

Evidence suggesting that a co-optimization of synaptic weights and delays can indeed achieve competitive performance on spatio-temporal classification problems, while simultaneously decreasing the number of training parameters in an SNN without loss of accuracy [17, 21, 22]. This finding is especially important for neuromorphic architectures that target limited resource scenarios.

Nevertheless, from an algorithmic perspective, optimizing delays in SNNs remains an ongoing research problem. Previous literature has largely focused on either exploiting heterogeneity in delay parameters, while limiting gradient-based training to the weights to “select” suitable delays [17, 22, 23], or using evolutionary, not gradient-based, algorithms to find delay parameters [24]. Recently, several approaches based on surrogate gradients [25] have been proposed, using convolutional kernels [21] or finite difference methods [18, 26]. However, these methods inherently rely on an approximation of the true gradient, which additionally requires access to neuronal membrane potentials for calculating parameter updates. Moreover, these algorithms operate in discrete time and require the storage of neuronal activities as binary vectors over the entire history of the SNN.

In addition, from a hardware perspective, there is a growing number of neuromorphic platforms that support the emulation of delays. These implementations require additional memory elements and parameter sets to retain the information of the incoming spike for a controllable amount of time. Previous implementations of on-chip delays using Complementary Metal-Oxide-Semiconductor (CMOS) technology have used digital circuits [22, 27–30], active analog circuits [31–34], or mixed-signal solutions [35]. Furthermore, emerging memory technologies such as Resistive Random Access Memory (RRAM) have also been used to realize delay elements, taking advantage of their non-volatile, small 3D footprint, and zero-static-power properties [17, 29]. This increasing abundance of neuromorphic substrates offering configurable delays reveals an implicit call for algorithms capable of exploiting these novel capabilities.

In this work, we present DelGrad, the – to our knowledge – first exact, analytical solution for gradient-based, hardware-compatible co-learning of delays and weights, using exclusively spike times for the computation of parameter updates. Compared to previous approaches, this simultaneously increases precision and computational efficiency, while also minimizing the required memory footprint. Under DelGrad, we quantitatively study the effect of different types of delays in relation to network performance and sizes. And, in a final step, we experimentally demonstrate our method’s amenability to implementation on mixed-signal neuromorphic platforms capable of emulating SNNs, even when their design does not include specific circuits for implementing spike timing delays.
2 Training delayed networks with exact error backpropagation

Spike time gradient of transmission delays We start by briefly reviewing the effect of transmission delays on the activity of a single LIF neuron with exponential current-based synapses. The time evolution of its membrane potential $u_m$ is governed by the differential equation

$$\tau_m \dot{u}_m(t) = [E_l - u_m(t)] + I_s(t)/g_L$$

(1)

with membrane time constant $\tau_m$, leak potential $E_l$, leak conductance $g_L$ and synaptic input current $I_s$. Synaptic kernels are assumed to be exponential with time constant $\tau_s$ and amplitude (weight) $w$. Upon crossing the threshold $\vartheta$, the membrane is reset to $E_l$ for a refractory period $\tau_{ref}$ and the neuron emits an output spike.

The response function of a neuron thus maps a sequence of input spike times $t_i$ to a sequence of output spike times $T_i$. For one such output spike time $T$, under a parameterization given by the synaptic weights $w_i$, we can write:

$$T = T(\{t_i\}; \{w_i\}) .$$

(2)

For certain integer ratios between time constants, the function $T$ becomes analytic, as discussed in [36]. For example, for $\tau_m = \tau_s$ one obtains

$$T = \tau_s \left\{ \frac{b}{a_1} - W\left[-\frac{g_L \vartheta}{a_1} \exp\left(\frac{b}{a_1}\right)\right]\right\} ,$$

(3)

and for $\tau_m = 2\tau_s$

$$T = 2\tau_s \ln \left[\frac{2a_1}{a_2 + \sqrt{a_2^2 - 4a_1g_L \vartheta}}\right] ,$$

(4)

where $a_1$ and $b$ are explicit functions of $w_i, t_i$ and $W$ is the Lambert W function (see Eq. (8)).

To compute the ultimately relevant gradients $\partial L/\partial \theta$ (for parameters $\theta \in \{w_i\} \cup \{d_i\}$) in the backward differentiation mode (as in error backpropagation), one needs to evaluate two types of gradients; with the above equations, these can be calculated analytically. $\partial T/\partial w_i$ allows us to link a deviation in an output spike time to a change in weight parameters, while $\partial T/\partial t_i$ relates this deviation in output to deviation in the input, thereby enabling us to propagate an error in the spike time backwards through the neuron.

Delays can now simply be introduced as additive parameters $d$ to the original spike times $t^d$:

$$t_i^d = t_i + d_i .$$

(5)

These delayed spike times then become the relevant input for the postsynaptic neuron. As above, derivatives of this expression provide the necessary quantities for adapting the delays and for backpropagating the spike timing errors. In this case, the corresponding equations are trivial:

$$\frac{\partial t_i^d}{\partial t_i} = 1 \text{ and } \frac{\partial t_i^d}{\partial d_i} = 1 .$$

(6)

We note that these considerations are not contingent on a specific network setup and thus apply to any activity patterns in arbitrary spiking networks. In the following, we focus our attention on the particular problem of pattern classification, for which we employ a specific network architecture and spike coding scheme (Fig. 1).

Extension to a multi-layer network To take advantage of a well-established architectural paradigm, we now consider information propagation in hierarchical feedforward networks. As also shown in the corresponding computational graph (Fig. 2a, solid black arrow), the input $t^0$ is passed through the sequence of layers until it reaches the output.\(^1\)

The gradient of the chosen loss function $L$ then goes backwards through the network (dashed red arrow) for optimizing the parameters. In the forward pass, the only information that is transmitted are spike times $t^1$; in the backward pass, we transmit the gradient of the loss function $\partial L/\partial t^1$, but note that it is also only evaluated at the times when neurons spike.

For SNNs with delays, the computational graph differentiates between two types of (virtual) layers: neuron layers and delay layers. Both layers receive input spikes $t^{l-1}$ and return output spikes $t^l$, but using different forward transfer

\(^1\)We use bold symbols to denote non-scalar variables.
Figure 2: **Computational graph of a multi-layer SNN with spike-time information encoding and adjustable delay and weight parameters.**

a) Graph for a multi-layer network with spike times $t^0$ injected into the bottom ($1^{st}$) layer. In the forward pass (black arrows), each layer $l$ takes spike times as inputs and returns spike times as outputs that go into the next layer. The spike times of the topmost layer are used to compute the loss function $L$. The backward pass (red dashed arrows) starts at the loss and passes the gradients backwards through the layers. We consider two types of layers: neuron layers and delay layers.

b) Neuron layer with parameters $w^l$ (synaptic weights). These are used together with the input spike times $t^{l-1}$ to calculate the output spike times $t^l$ according to Eqs. (3) and (4).

c) Delay layer with parameters $d^l$ that are simply added to the input spike times $t^{l-1}$ to calculate the output spike times $t^l$ as in Eq. (5).

functions, as given by Eq. (3)/Eq. (4) and Eq. (5), respectively. In the backward direction, they pass the partial derivative $\partial L/\partial t^{l-1}$ discussed above. Figure 2b and c highlight the similarity of the two layer types, neuron and delay, in this setup they both take spike trains as an input and produce spike trains as an output in the forward pass, and propagate gradients of the loss with respect to the corresponding spike times in the backward pass. Their respective computations are carried out sequentially, as depicted in Fig. 2a, with delay layers stacked in between neuron layers.

**Delay implementation**

In Fig. 3a we distinguish between different types of delays: axonal delays $d_{\text{axo}}$ on a neuron’s output, dendritic delays $d_{\text{den}}$ on a neuron’s input, and synaptic delays $d_{\text{syn}}$ that are specific for every connection between pairs of neurons. Their respective natural representations as column vectors, row vectors and matrices are shown in Fig. 3b. The memory footprint of axonal and dendritic delays thus scales linearly with the number of neurons in the network, while for synaptic delays, it scales linearly with the network depth and quadratically with its width.

While in principle different types of delays can be simultaneously present in a network and can be combined with each other, it is important to note that, as illustrated in Fig. 3c, combining dendritic and axonal delays for the same neuron is redundant: as neuronal dynamics are invariant to temporal shifts, it is equivalent whether inputs arrive with a delay $d_{\text{den}} = d$, thereby causing delayed output spiking (red arrow and gray curve), or whether the output of the neuron is directly delayed with $d_{\text{axo}} = d$ (orange arrow and membrane dynamics in black).

Given the resource constraints of neuromorphic systems, it is particularly relevant to specifically investigate the performance benefits incurred by the different delay types, which we do in the following sections. Regarding their hardware footprint, a quantitative evaluation of their energy consumption, required chip area and design complexity depends heavily on both the entirety of the chip’s architecture, the chosen design principles (e.g., analog vs. digital components) and the design choices for the delay mechanism itself. Nevertheless, some generic statements can be made, which mirror the conclusions drawn above from the abstract mathematical structures employed for the representation of the different delay types. For typical crossbar architectures (Fig. 3d), the synaptic delay mechanisms are most likely located within the crossbar array and therefore scale with the product of pre- and post-synaptic neuron numbers. In contrast, dendritic and axonal delays can be located in the vicinity of the neurons and their number (and area) thus
Figure 3: **Illustrating different types of delays.** a) From bottom to top: axonal delays shift the timing of the neuron’s outgoing spikes by \( d_{axo} \) (orange); synaptic delays shift the timing of spikes by a specific value \( d_{syn} \) for each pair of pre- and post-synaptic neuron (purple); dendritic delays shift the timing of the incoming spikes into a neuron by \( d_{den} \) (red). b) Vector and matrix representation of the different types of delays and their dimensionality as a function of the number of pre- and post-synaptic neurons. c) Equivalent effect of the dendritic and axonal delays on the output spike time of a neuron, due to the time-shift invariance of the temporal dynamics of a LIF neuron. d) Schematic illustration of the location of synaptic, dendritic and axonal delay components in a generic neuromorphic crossbar architecture.

scales linearly with the number of neurons in the network. However, an important property of axonal delay mechanisms is that they are located directly after the neurons’ output and therefore only need to operate on sparse events. In contrast, dendritic delays are located directly before then neurons’ input, and after the input signals have been scaled by the synaptic elements.

Depending on the design choices, in particular on whether the synaptic convolution happens in the synapses or in the neurons, this may require more complex circuitry. Note also that neurons usually receive more spikes than they emit, so the required buffering may also increase the corresponding hardware footprint of dendritic delay implementations.

3 Simulation

**Setup** In this section, we benchmark a PyTorch [38] implementation of the DelGrad method using the YY [37] dataset, to evaluate the impact of transmission delays on the SNN performance, and assess how this varies with the network size.

This dataset is selected for its advantageous properties – compactness, training speed, and discriminatory power between network architectures and training paradigms. The task is to classify the region of a Yin-Yang image to which a point in the image plane belongs, as illustrated in Fig. 4a. The coordinates of the point \((x, y)\) and their mirrored values \((1 - x, 1 - y)\) are encoded into spike times, such that a larger value of the coordinate results in a later spike time, and an early spike time for its mirrored version.

The network architecture is a feed-forward multi-layer configuration with four input neurons, followed by a variable-size hidden layer and finally an output layer, comprising three neurons for the three classes (see Fig. 1). Optionally, delay layers may be inserted between neuron layers, as previously illustrated in the computational graph (Fig. 2). The neurons have no configurable biases, and the time constants are configured such that \( \tau_m = 2\tau_s \). Thus, we utilize Eq. (4) for training. The refractory period \( \tau_{ref} \) is set to infinity, such that all neurons only spike once. The output is represented in a time-to-first-spike (TTFS) decoding scheme, where the first output neuron to spike indicates the predicted class for a given input.

To avoid negative or excessively large values for the delays, a regularization strategy is implemented. The effective delay \( d \) is calculated as a logistic function of a trainable parameter \( \theta_d \) such that \( d = \sigma(\theta_d) \), which ensures that the delays remains bounded between 0 and 1.
Figure 4: Classification task and simulation results. a) The Yin-Yang (YY) task [37] consists of the classification of dots based on whether they belong to the Yin (red), Yang (blue), or dot (green) regions, as illustrated in 4a. The input features are the two dimensional coordinates \((x, y)\) of the image, along with their mirrored values \((1-x, 1-y)\), totaling four features. These features are encoded into spike times, such that a larger value of \(x\) or \(y\) coordinate results in a later spike time for \(x\) or \(y\) and an early spike time for its mirrored version \(1-x\) or \(1-y\) respectively. For more details on the encoding, see the original publication. b) Test error as a function of the number of hidden neurons in an SNN, using different delay types. The solid lines and markers show the median of the error, and the shaded areas illustrate the interquartile ranges (IQRs) for 25 seeds. c) Same data as in b) but as a function of the number of trainable parameters in the networks, i.e., counting the distinct weights and, if applicable, delays.

To improve performance and stabilize training, we find that a time-invariant mean squared error (MSE) loss works best:

\[
\mathcal{L}_{\Delta \text{MSE}}[t, n^*; \Delta_t] = \frac{1}{2} \sum_{n \neq n^*} [(t_n - t_{n^*}) - \Delta_t]^2 ,
\]

where \(n^*\) and \(n\) denote the respective indices of the correct and wrong label neurons and \(\Delta_t\) is a freely choosable parameter. Instead of providing target spike times, this loss function tries to achieve a specific separation of \(\Delta_t\) between the spike times of the correct and incorrect label neurons. To ensure a balance between model accuracy and hardware compatibility, \(\Delta_t\) is set to 0.2\(\tau_s\) in our simulations.

Results We investigate the effects of different types of delay layers on accuracy, including configurations without any delays. Figure 3 reports the performance of our approach on the YY dataset across different network sizes. Optimal learning rates are determined through hyper-parameter optimization for each configuration of neuron and delay layers. Across all investigated settings, our approach demonstrates robust training convergence (see also Fig. SI.1 for further simulation results). Fig. 4b shows that co-training delays alongside the weights always improves performance, regardless of the specific type of delay. Among the delay-augmented configurations, the variant with synaptic delays outperforms the ones with axonal- or dendritic-only parameters.

Fig. 4c displays the same test errors, but now as a function of the number of parameters. This representation reveals that, at least for the YY dataset, delay-augmented networks with the same number of parameters perform similarly well, regardless of the type of delay. As before, for a given number of parameters, the co-training of delays always yields at least as good results as the training of synaptic weights alone. In other words, for the same memory footprint, a mix of both weights and delays is better than just synaptic weights. Overall, these results clearly evince the added value of learning delays, as well as the ability of our algorithm to capitalize on this potential.
Figure 5: **Proof of concept for implementing on-chip axonal delays on BrainScaleS-2.**

- **a)** Photograph of the BrainScaleS-2 neuromorphic chip (taken from [39]).
- **b)** Schematic illustration of the network architecture for on-chip axonal delays; here, we apply this generic approach to the BrainScaleS-2 neuromorphic hardware. Each neuron in the network is paired with a parrot neuron connected in a one-to-one scheme. The parrot neuron repeats each of its input spikes with a configurable delay.
- **c)** Example membrane trace of a parrot neuron where the rise time of the PSP causes a delay of its output spike with respect to the output spike time of its afferent network neuron. This delay can be configured through an appropriate choice of the synaptic weight between network neuron and parrot neuron.
- **d)** Example BrainScaleS-2 recording of the relationship between the measured input-output delay of a parrot neuron $d_{\text{rec}}$ and its afferent synaptic (neuron 3 in f)). Mean and standard deviation are shown over 10 runs with 50 spike pairs each. An exponential fit (black) yields the calibration curve for the weight-delay relationship.
- **e)** Test of the calibration for the same parrot neuron as in d). The calibration curve from the fit in d) is used across a range of target delays $d_{\text{tgt}}$ to determine the corresponding optimal synaptic weights. With this weight the delay is re-measured for 5 runs with 50 spike pairs each, checking the deviation between the predicted delay (black) and the actually recorded delay $d_{\text{rec}}$ (mean and standard deviation in blue).
- **f)** Same as e) but for 5 different parrot neurons on the chip to illustrate the variability between different neuron circuits.

## 4 Hardware results

As DelGrad only requires spike times as observables, it is ideally suited for implementation on a variety of neuromorphic substrates. Here, we demonstrate the flexibility of our method by describing a successful application in silico, even on a neuromorphic platform that does not natively support delays: BrainScaleS-2 (BSS-2).

The BSS-2 system (Fig. 5a, [7, 40]) is built around a mixed-signal neuromorphic chip with 512 physical neuron circuits. The neuron dynamics are accelerated compared to biological time scales by a factor of $10^3$. The neuron circuits emulate the dynamics of the adaptive exponential leaky integrate-and-fire (AdEx) model with individually configurable parameters for each neuron. Both current-based and conductance-based exponential synaptic inputs are available. Here, we choose the current-based variant and parametrize the AdEx neurons such that their dynamics follow the LIF model. The connectivity between the neurons on the chip can be configured arbitrarily within the constraints of the two $256 \times 256$ synaptic crossbar arrays. The synaptic weights are configured digitally with 6 bit resolution.

Despite the current generation of BSS-2 not natively supporting delays, we present two approaches to explore the computational potential of delays on the current substrate. First, we show how one can emulate analog axonal delays on-chip by re-purposing a subset of the available neurons as delay elements. Second, we perform in-the-loop training of networks with axonal delays in a hybrid hardware-software approach. For that, we emulate neurons and synapses on-chip while applying the delays digitally off-chip.
4.1 Proof of concept for axonal on-chip delays

Setup Even without "true" delays, an effective axonal delay can be achieved by exploiting the dynamics of the analog on-chip neuron circuits. For that, a "parrot neuron" is connected, with a configurable weight, to the output of a neuron that is part of the actual trained network (Fig. 5b). For any spike that the network neuron produces, the parrot neuron is configured to also output a spike. Due to the finite rise time of the PSP on the parrot’s membrane voltage, this spike is delayed compared to the one of the network neuron (Fig. 5c). The magnitude of this delay, which emulates the axonal delay of the network neuron, depends on several parameters, such as the synaptic weight \( w \) of the connection between the network and parrot neurons, the time constants \( r_s, r_m \) and the difference between threshold and leak potential of the parrot neuron.

For our implementation of this scheme on BSS-2, we control the delay solely via the synaptic weight \( w \), while keeping the time constants and potentials fixed (though individually calibrated for every neuron). A more detailed description of our setup and design choices can be found in Appendix SI.C. Since in our trained networks on BSS-2 ([36] and Section 4.2) we use neuron time constants of \( r_s = r_m \approx 6\mu s \), we aim to reach delays of the same magnitude here.

During the training of a network, it is required to reconfigure the parrot neurons on the chip to produce the axonal delays \( d_{\text{axo}}^{\text{tgt}} \) as prescribed by the learning algorithm. For this, the relationship between the synaptic weight \( w \) and the produced delay \( d_{\text{rec}} \) needs to be measured. Due to the usual variations in the manufacturing process (fixed-pattern noise), the on-chip analog neuron circuits are not exactly identical to each other. Therefore, for every parrot neuron, we perform a separate calibration measurement in order to determine the precise mapping between the weight parameter and the recorded delay individually. To this end, we configure a range of different weights, record the resulting delays \( d_{\text{rec}} \) (Fig. 5d for an example neuron), and fit an exponential function to this data. The inverse of the fit function thus determines the relation between the target delay \( d_{\text{axo}}^{\text{tgt}} \) and the optimal integer weight to configure on the chip. To test the quality of the weight-delay fit, it is used to configure the chip for a whole range of target delays \( d_{\text{axo}}^{\text{tgt}} \), while measuring the actual value of the delays produced on the chip \( d_{\text{axo}}^{\text{rec}} \). The above process is repeated for 5 different neuron circuits on the chip, and the results are compared to illustrate the impact of fixed-pattern noise in Fig. 5f.

Results Figure 5e shows the desired correspondence between the target, \( d_{\text{axo}}^{\text{tgt}} \), and the recorded, \( d_{\text{axo}}^{\text{rec}} \), on-chip delay values, especially in the intermediate delay range. This underpins the feasibility of our proposed approach. However, two additional remarks are in order. First, we note a plateau in the recorded delay values for lower targets, caused by the maximum possible on-chip weight value, corresponding to the shortest possible delay. Second, a larger deviation and more instability is observed for larger target delays; this effect has two causes: a worse quality of the exponential fit and an increased instability of the threshold crossing in the region where the PSP plateaus. Such increasing instability is unavoidable in analog neurons, as any amount of noise on the membrane voltage results in increased trial-to-trial variability when the peak of the PSP is close to the threshold.

Although each neuron can be configured individually to produce the desired behavior, there is still some variability between the neurons. However, we do not expect these variations to be harmful in practice; in fact, some heterogeneity between neurons behavior might even be beneficial, as has been shown in [13]. These results provide a proof of concept that axonal delays can be implemented by repurposing resources and circuits that are universally available on any neuromorphic substrate. Nevertheless, while the presented idea can be feasible for small networks and tasks, it is clearly sub-optimal, as it requires a portion of the available neuron circuits to be used as delay elements instead of their usual role in the network. Additionally, several practical considerations have to be taken into account when this setup is included in the training of a full network. First, the range of achievable delays is limited by the time constants of the parrot neurons. In our experiments we targeted a delay range of approximately 6\( \mu s \) which corresponds to the delay range used in the results in Sections 3 and 4.2. But different tasks might require a larger range of delays. To address this, the circuitry of the exponential and adaptation terms in the AdEx neurons on BSS-2 could potentially be used to increase the delay range and stabilize the increased trial-to-trial variability for larger delays. Second, for a correct delay on an incoming spike, the parrot neuron’s membrane voltage and synaptic currents need to be at their resting values. Therefore, the interval between spikes arriving at the parrot neuron needs to be large enough, which can be ensured by increasing the refractory time of the neurons in the network. However, for tasks where the neurons need short refractory periods to process their input correctly, this method of producing axonal delays is not suitable.
4.2 In-the-loop training with off-chip delays

Setup  In addition to our proof-of-concept demonstration of analog axonal delays, we also employ our training method in a setting where delays are generated digitally. However, since BSS-2 does not include a digital infrastructure to produce such delays, we use off-chip delays generated by the host as a proxy. This enables the implementation of delays in a multi-layered network with high precision. Figure 6a and b illustrate this method for a network with a hidden and an output layer that are emulated in consecutive passes on the chip (but without any reset or reconfiguration). In between the passes, the recorded spikes of the neuron on the chip are sent to the host, the delays are applied in software, after which the spikes are sent back to the chip as input for the next layer. Although in principle this setup is suitable for all delay types (dendritic, axonal or synaptic), we choose axonal delays in our experiments for simplicity.

We employ an in-the-loop training mechanism, where for every batch, the neurons and synapses are emulated on the chip, from which the spikes are read out, and the resulting gradient and weight updates are calculated on the host computer. The updated weights are programmed back to the chip and the process is repeated with a new training batch. For more details on the training procedure, as well as the mapping of an Fast&Deep (FnD) network onto BSS-2, we refer to the methods section of [36]. Note that, similar to [36], we choose the configuration of $\tau_s = \tau_m$, while for the simulations in Section 3, there is a factor of two between the time constants.

Due to the low input dimensionality of the YY dataset, the synaptic weights between the input and hidden layer need large on-chip weight values in order to elicit spikes in the hidden neurons. Due to the limited weight range on the hardware, this effectively reduces the range of available on-chip weight values for learning. To avoid this, we follow [36] and copy each input channel 5 times and feed each spike into the chip via a distinct input channel. This effectively increases our input dimension to 20. While this does not provide any computational advantage in a setup without delays, as the weights from the copied channels just sum linearly, axonal delays of the input channels can learn to exploit this multiplexing. This results, for our input layer, in a similar setup as described in Fig. 1B of [23], with the added benefit of the delays being adjustable and not just selectable.
Results

With this setup, we can train and compare networks with only synaptic weights and networks with adjustable weights and axonal delays (Fig. 6c and d). Similar to the results in Fig. 4, we observe an accuracy gain, over a range of network sizes, for the networks with additional delay parameters, compared to the ones with only weight parameters. Here, the performance gap between the delay and no-delay setup appears to be wider. This could partially be explained by the additional computational power that a delay setup can gain from the input multiplexing, as well as the general advantage of increased computational power through delays.

While still preliminary, these results already show the benefit of learnable delays for neuromorphic platforms, especially in resource-constrained scenarios, and might encourage the inclusion of delay mechanisms in future hardware generations.

5 Discussion

We have proposed an efficient gradient-based algorithm for training temporal variables, specifically transmission delays in SNNs alongside synaptic weights, and have experimentally demonstrated its capabilities both in software simulations and on neuromorphic hardware. Delay parameters were previously demonstrated to increase the representational power of the SNNs, even without adapting them, just by training the weight parameters to select the useful delays for spatio-temporal feature detection [17, 22]. However, this optimization-through-selection approach requires an overallocation of resources in order to provide a sufficiently diverse set from which the best delay can be selected. We propose that a more efficient solution can be provided by combining a dedicated learning algorithm for transmission delays with hardware capable of configuring them accordingly.

Algorithms based on surrogate gradients for direct training of delay elements have been explored recently, using temporal convolution kernels [21] or numerical solutions that estimate the delay gradients using finite-difference approximations [18]. However, as pointed out in [21], the finite-difference approximation appears to not be sufficiently accurate to achieve an improvement over fixed, random delays. Additionally, both approaches use a time-stepped framework for calculating the surrogate gradients.

As such, delays are represented implicitly in the number of simulation time steps before transmitting a spike. However, as delay parameters are essentially shifts in individual spike times, we argue that it is more natural to have a framework where the information is explicitly represented by these spike times [29, 36], and delays are learned as additive parameters for these times. Furthermore, the objective of building efficient asynchronous neuromorphic systems, where time represents itself, is an additional motivation for representing temporal information in spike times [3]. Such representations are naturally available from event-based sensors, where the change in the signal is encoded into spike times using the delta modulation encoding scheme [41–43].

This work brings together all the aforementioned objectives: DelGrad presents an event-based framework for gradient-based co-training of delay parameters and weights, without any approximations, and which meets the typical demands and constraints of neuromorphic hardware, as demonstrated experimentally on an analog mixed-signal neuromorphic system. As such, it takes an important step towards fully exploiting the temporal nature of SNNs for memory- and power-efficient end-to-end event-based neuromorphic systems.

Different delay types and hardware considerations

In this work, we have also compared the effect of dendritic, axonal and synaptic delays on the performance of SNN on a representative task. The synaptic delays have the highest impact on increasing the expressivity of SNNs, compared to using only dendritic or axonal delays. However, from a hardware perspective, the addition of synaptic delays imposes a quadratic growth on the size and thus the on-chip area of the network, compared to a linear growth in the case of axonal and dendritic delays. In fact, we find that when comparing the performance for equal parameter counts, the gap between different types of delays vanishes while the superiority over weight-only training persists. As memory represents one of the most critical constraints in the design of neuromorphic, or generally Artificial Intelligence (AI) hardware, reducing on-chip memory is of utmost importance. Therefore, our work suggests that it might be practical to only consider using dendritic or axonal delays in future hardware designs, in order to combine favorable scaling and improved processing power.

Hardware mapping

DelGrad provides an advantage in terms of hardware mappability, especially in a chip-in-the-loop training scheme, as it only requires recording the spike times from on-chip neurons. This is in contrast to other approaches [18, 21], which require recording the full membrane potential of the neurons for surrogate gradient learning [44, 45]. Recording the membrane potential of all neurons, regardless of digital and analog design, requires vastly
more peripheral circuitry, with multiplexed readout mechanisms, which makes the system much more complicated, while also slowing down the chip-in-the-loop training.

**Outlook**  In this work, we have used the Yin-Yang dataset as a first step and proof of concept to benchmark our approach. The Yin-Yang dataset provides a non-linearly-solvable problem, where the information can be presented using a TTFS encoding, similar to the previous work [36].

The natural next step will reside in a more thorough benchmarking on various temporal datasets [46, 47], especially as provided by event-based sensors, where TTFS might reach its limits as a feasible coding scheme. Here, it will become important that although our current implementation only takes into account a single spike per neuron during the training, this is not a limitation of our proposed mathematical framework and training scheme. Additionally, the extension to more complex spike timing codes can go hand in hand with a shift from a feedforward to a recurrent network architecture.
References

11.  


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Supplementary Information

SI.A Additional equations for Section 2

Given a sequence of input spikes \( \{t_i\} \) and weights \( w_i \), we define

\[
a_n := \sum_{i \in C} w_i \exp \left( \frac{t_i}{\tau} \right) \quad \text{and} \quad b := \sum_{i \in C} w_i \frac{t_i}{\tau} \exp \left( \frac{t_i}{\tau} \right),
\]

for Equations (3) and (4). These definitions use the causal set \( C = \{i \mid t_i < T\} \) of input spikes before the output.

The Lambert W function is defined as the solution \( h = W(z) \) to the equation \( z = h \exp(h) \).

SI.B Extended simulation results

![Figure SI.1: Extended simulation results. a) Comparison of the validation error during training for the different delay types and a network without delays. All networks have one hidden layer with 30 neurons.](image)

SI.C Implementation details for on-chip axonal delays on BrainScaleS-2

As BrainScaleS-2 (BSS-2) does not include dedicated circuitry for emulating delays, we re-purpose neuron circuits to act as delay elements (parrot neurons, see Fig. 5b, c). For any incoming spike the parrot neuron is configured to produce an output spike. In principle, the delay with which the parrot neuron produces an output spike after receiving an input is controlled by the parrot’s time constants, the resting potential, the threshold and the synaptic weight.

For our implementation, however, we choose to control the delay solely via the synaptic weight \( w \), while keeping all other parameters fixed. This is because the time constants and potentials are analog parameters, which can be individually configured for each neuron, but the configuration of an analog parameter is slower than the configuration of the digital weight parameter. Therefore, for fast reconfigurations of the delays during training, we only modify weights.

For axonal delays in the desired range of up to 6\( \mu \)s, we configure the parrot neurons to have a synaptic time constant of \( \tau_s = 10 \mu s \) and a membrane time constant of \( \tau_m = 15 \mu s \). A long refractory time of 16\( \mu s \) ensures that each input to the parrot only triggers one output spike.

To determine the relationship between the synaptic weight and the delay, we sequentially configure a range of different weights and record, for each, the resulting delay \( d_{axo}^{rec} \) (Fig. 5d). Not the full weight range from 0 to 63 is
used, as for lower weights the parrot does not reliably produce output spikes. To include both temporal drift during one trial as well as trial-to-trial variations, we record delays during 10 runs with 50 pairs of input and output spikes and average the results. We fit an exponential function $d(w) = \alpha + \beta \exp(\gamma(w + \delta))$ to the measured data. The inverse of that fit gives us the relation to determine for any target delay $\theta_{tgt}$, the optimal integer weight to configure on the chip (Fig. 5e).

SI.D Explicit, event-based gradients of a voltage-max-over-time loss

Typically, when using an event-based framework, we try to encode information in networks in spike times. For some tasks, losses based on the voltage of (a subset) of neurons have been proposed and used, especially the max-over-time loss (for a selection, see [12, 44, 45]). The corresponding function is defined dependent on the correct class $n^*$ and voltage values in the label layer $u(t)$ together with a scale factor $\alpha$ as

$$L_{\text{MOT}}[u(t), n^*; \alpha] = - \log \left[ \text{softmax}_n(\alpha \cdot \max_t u(t)) \right].$$

The interesting derivative is the one of the maximum voltage $u_{\text{max}} := \max_t u(t)$ wrt. the parameters. For this, we look at a single voltage $u_{\text{max}}$ and define the time of maximum voltage $\tilde{t}$ through

$$\tilde{t} \text{ s.t. } u_{\text{max}} = u(\tilde{t}).$$

Now, we investigate $\frac{\partial u(t)}{\partial w_j} \bigg|_{t=\tilde{t}}$ in two different settings, starting with the more peculiar one.

Equal time constants $\tau_s = \tau_m$. In this regime the voltage behaves as

$$u(t) = \frac{1}{C_{\text{mem}}} \sum_i w_i \theta(t - t_i)(t - t_i) \exp \left( -\frac{t - t_i}{\tau_s} \right).$$

We can calculate the derivative to be

$$\left. \frac{\partial u(t)}{\partial w_j} \right|_{t=\tilde{t}} = \frac{1}{C_{\text{mem}}} \sum_i \frac{\partial w_i}{\partial w_j} (\tilde{t} - t_i) \exp \left( -\frac{\tilde{t} - t_i}{\tau_s} \right)$$

$$= \frac{1}{C_{\text{mem}}} \delta_{t_j < \tilde{t}} (\tilde{t} - t_j) \exp \left( -\frac{\tilde{t} - t_j}{\tau_s} \right).$$

Similarly we get

$$\left. \frac{\partial u(t)}{\partial t_j} \right|_{t=\tilde{t}} = \frac{1}{C_{\text{mem}}} \delta_{t_j < \tilde{t}} w_j (\tilde{t} - t_j - \tau_s) \exp \left( -\frac{\tilde{t} - t_j}{\tau_s} \right).$$

Unmatched time constants $\tau_s \neq \tau_m$. While the voltage dynamics is slightly different

$$u(t) = \frac{1}{C_{\text{mem}}} \frac{\tau_m \tau_s}{\tau_m - \tau_s} \sum_i w_i \theta(t - t_i) \left[ \exp \left( -\frac{t - t_i}{\tau_m} \right) - \exp \left( -\frac{t - t_i}{\tau_s} \right) \right],$$

the calculation is very similar and results in

$$\left. \frac{\partial u(t)}{\partial w_j} \right|_{t=\tilde{t}} = \frac{1}{C_{\text{mem}}} \frac{\tau_m \tau_s}{\tau_m - \tau_s} \delta_{t_j < \tilde{t}} \left[ \exp \left( -\frac{\tilde{t} - t_i}{\tau_m} \right) - \exp \left( -\frac{\tilde{t} - t_i}{\tau_s} \right) \right],$$

$$\left. \frac{\partial u(t)}{\partial t_j} \right|_{t=\tilde{t}} = \frac{1}{C_{\text{mem}}} \frac{\tau_m \tau_s}{\tau_m - \tau_s} \delta_{t_j < \tilde{t}} \left[ \frac{1}{\tau_m} \exp \left( -\frac{\tilde{t} - t_j}{\tau_m} \right) - \frac{1}{\tau_s} \exp \left( -\frac{\tilde{t} - t_j}{\tau_s} \right) \right].$$

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